CLAIMS:

1. A chip stack comprising:

a flex circuit comprising:

a flex substrate;

a first conductive pattern disposed on the flex substrate; and

a plurality of leads extending from the flex substrate and electrically connected to the first conductive pattern;

at least two integrated circuit chip packages electrically connected to the first conductive pattern.

2. The chip stack of Claim 1 wherein:

the flex substrate defines opposed top and bottom surfaces; and

the first conductive pattern comprises:

a first set of flex pads disposed on the top surface of the flex substrate; and

a second set of flex pads disposed on the bottom surface of the flex substrate;

the flex pads of the first and second sets being electrically connected to the leads, with one of the integrated circuit chip packages being disposed upon the top surface of the flex substrate and electrically connected to at least some of the flex pads of the first set and one of the integrated circuit chips being disposed upon the bottom surface of the flex substrate and electrically connected to at least some of the flex pads of the second set.

3. The chip stack of Claim 2 wherein the flex pads of the first and second sets are arranged in identical patterns.

4. The chip stack of Claim 2 wherein:

the flex substrate has a generally rectangular configuration defining opposed pairs of longitudinal and lateral peripheral edge segments; and

the leads extend from at least one of the longitudinal and lateral peripheral edge segments of the flex substrate.

5. The chip stack of Claim 1 wherein each of the leads is an S-lead.

6. The chip stack of Claim 2 wherein the integrated circuit chip packages each comprise:

a package body having opposed, generally planar top and bottom surfaces; and

a plurality of conductive contacts disposed on the bottom surface of the package body;

the conductive contacts of one of the integrated circuit chip packages being electrically connected to respective ones of the flex pads of the first set, with the conductive contacts of one of the integrated circuit chip packages being electrically connected to respective ones of the flex pads of the second set.

7. The chip stack of Claim 6 wherein the flex pads of the first and second sets and the conductive contacts are arranged in identical patterns.

8. The chip stack of Claim 6 wherein each of the integrated circuit chip packages comprises a CSP device.

9. The chip stack of Claim 8 wherein the integrated circuit chip packages are each selected from the group consisting of:

a BGA device;

a fine pitch BGA device; and

a flip chip device.

10. A chip stack comprising:

a flex circuit comprising:

a flex substrate;

a first conductive pattern disposed on the

flex substrate; and

a plurality of conductive leads extending from the flex substrate and electrically connected to the first conductive pattern;

at least two integrated circuit chip packages, one of the integrated circuit chip packages being electrically connected to the first conductive pattern, with one of the integrated circuit chip packages being attached to the flex substrate in non-conductive contact therewith.

11. The chip stack of Claim 10 wherein:

each of the integrated circuit chip packages includes a plurality of conductive contacts; and

the first conductive pattern of the flex circuit and the conductive contacts of the integrated circuit chip package attached to the flex substrate in non-conductive contact therewith collectively define a composite footprint of the chip stack which is electrically connectable to another component.

12. The chip stack of Claim 10 wherein:

the flex substrate defines opposed top and bottom surfaces; and

the first conductive pattern comprises:

a first set of flex pads disposed on the top surface of the flex substrate and electrically connected to respective ones of the leads;

one of the integrated circuit chip packages being disposed upon the top surface of the flex substrate and electrically connected to at least some of the flex pads of the first set, with one of the integrated circuit chip packages being attached to the bottom surface of the flex substrate.

13. The chip stack of Claim 12 wherein:

the flex substrate has a generally rectangular

configuration defining opposed pairs of longitudinal and lateral peripheral edge segments; and

the leads extend from at least one of the longitudinal and lateral peripheral edge segments of the flex substrate.

14. The chip stack of Claim 10 wherein each of the leads comprises an S-lead.

15. The chip stack of Claim 10 wherein each of the leads comprises a J-lead.

16. The chip stack of Claim 12 wherein the integrated circuit chip packages each comprise:

a package body having opposed, generally planar top and bottom surfaces; and

a plurality of conductive contacts disposed on the bottom surface of the package body;

the conductive contacts of one of the integrated circuit chip packages being electrically connected to respective ones of the flex pads of the first set, with the top surface of the package body of one of the integrated circuit chip packages being attached to the bottom surface of the flex substrate.

17. The chip stack of Claim 16 wherein the flex pads of the first set and the conductive contacts are arranged in identical patterns.

18. The chip stack of Claim 16 wherein the package body of one of the integrated circuit chip packages is attached to the bottom surface of the flex substrate via an adhesive layer.

19. The chip stack of Claim 16 wherein the integrated circuit chip packages each comprise a CSP device.

20. The chip stack of Claim 19 wherein the integrated circuit chip packages are each selected from the group consisting of:

a BGA device;

a fine pitch BGA device; and

a flip chip device.

21. The chip stack of Claim 16 wherein the leads and the conductive contacts of the integrated circuit chip package attached to the bottom surface of the flex substrate are arranged to collectively define a composite footprint electrically connectable to another component.

22. A method of assembling a chip stack, comprising the steps of:

a) providing a flex circuit having a flex substrate defining opposed top and bottom surfaces, a first conductive pattern disposed on the flex substrate, and a plurality of leads extending from the flex substrate and electrically connected to the first conductive pattern;

b) positioning a pair of integrated circuit chip packages upon respective ones of the top and bottom surfaces of the flex substrate; and

c) electrically connecting the integrated circuit chip packages to the first conductive pattern of the flex circuit.

23. A method of assembling a chip stack, comprising the steps of:

a) providing a flex circuit having a flex substrate defining opposed top and bottom surfaces, a first conductive pattern disposed on the flex substrate, and a plurality of leads extending from the flex substrate and electrically connected to the first conductive pattern;

b) positioning a first integrated circuit chip package upon the top surface of the flex substrate;

c) electrically connecting the first integrated circuit chip package to the first conductive pattern; and

d) attaching a second integrated circuit chip

package to the bottom surface of the flex substrate.

24. The method of Claim 23 wherein step (d) is accomplished through the use of an adhesive.

25. The method of Claim 23 wherein step (d) comprises orienting the second integrated circuit chip package upon the bottom surface such that the second integrated circuit chip package and the leads of the flex circuit collectively define a composite footprint electrically connectable to another component.